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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/670,716	09/25/2003	David A. Luick	ROC920030300US1	6096

7590 12/22/2006

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EXAMINER	
CHU, GABRIEL L	
ART UNIT	**PAPER NUMBER**
2114	

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	12/22/2006	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary	Application No.	Applicant(s)	
	10/670,716	LUICK, DAVID A.	
	Examiner	Art Unit	
	Gabriel L. Chu	2114	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *25 September 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-18* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-18* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *25 September 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claim Objections

1. Claim 18 objected to because of the following informalities:

Referring to claim 18, "the area" has no antecedent basis. It is understood to refer to "an area".

Appropriate correction is required.

Claim Rejections - 35 USC § 112

2. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

3. Claims 1-18 rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

4. Referring to claims 1, 11, 18, and subsequently claims 2-10, 12-17, the claims claim an area "defined"/"covers" by "at most" a plurality of data paths. It is not clear how computing units can be placed in this same area if the area may only be "at most" (by the strictest interpretation) only the area that the data paths cover. Applicant is reminded that the area between the data paths is not covered by such a strict interpretation. Applicant is intending computing units to be such as that disclosed by elements 208 and 210, which perform multi-bit operations of addition, ALU, and rotation. Such operations require the passing of information between bit operators. See for example, the cited references from Wikipedia and a college-level project for ALU layout.

Applicant should note, for example, the use of a carry. While, as indicated in Applicant's background, it is known for FET logic to occupy an area within a wire width, Applicant does not appear to take into account the perpendicular movement of data between elements that is necessary to accomplish computation, particularly of the ALU, adder, and rotator types. In view of this shortcoming, it is not clear what such "at most" area is intended to cover. For the purpose of examination such area is interpreted as an area containing such data paths.

5. Referring to claim 18, while Applicant has shown data path means for a plurality of data paths, it is not clear to what means Applicant refers when claiming "means for devising a plurality of data paths". Further, this does not appear to coincide with what Applicant has claimed in claims 1-17. For the purpose of examination, claim 18 is understood to refer to "a plurality of data path means for connecting..." and "...being placed within an area defined by the plurality of data path means".

Claim Rejections - 35 USC § 102

6. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> **A person shall be entitled to a patent unless –**
>
> **(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.**

7. Claims 1, 2, 4-6, 8, 10-14, 18 rejected under 35 U.S.C. 102(e) as being anticipated by US 6697979 to Vorbach et al.

8. Referring to claim 1, Vorbach discloses a runtime repairable processor within a single silicon chip, comprising:

a plurality of data registers (From line 44 of column 11, "Before executing the test algorithms, the internal registers of the cells (1702) are stored in the RAM or RAM area (1701). After execution of the test algorithms, the data is written back into the internal registers of the cells.");

a first computing unit (From line 44 of column 12, "PAE: processing array element according to German Patent Application No. 196 51 075.9-53. Although a PAE in German Patent Application No. 196 51 075.9-53 is an arithmetic and logic unit, the term is used in more general terms in the present patent to represent any desired cell, i.e., arithmetic and logic units, state machines, memories, etc.");

an area of the silicon chip defined by at most a plurality of data paths for connecting the plurality of data registers to the first computing unit (For example, figure 1, buses 0110 and PAEs 0101.);

and a second computing unit, wherein the second computing unit is a duplicate of the first computing unit and is connected to the plurality of data registers (From line 50 of column 12, "PAER: cell which is additionally implemented on the integrated circuit and can be used as a replacement for a defective cell of the same design."), the first computing unit and the second computing unit being placed within the area (For example, figure 1, PAEs 0101 are within an area defined/covered by the buses 0110.).

9. Referring to claim 2, Vorbach discloses an enabling control logic, wherein the enabling control logic disables the first computing unit and enables the second computing unit when a failure is detected with the first computing unit (Figure 1, 0109.).

10. Referring to claim 4, Vorbach discloses a machine state register including a unit selecting indicator, the unit selecting indicator controlling the enabling control logic (Figure 1, 0109.).

11. Referring to claim 5, Vorbach discloses the unit selecting indicator is set by software (From line 12 of column 5, "Another possibility is the fixed integration of test strategies into the application programs to perform tests during processing of the application program. In both cases, the relevant data in the array is saved before calling up the test algorithms. One option is to save the data either in internal memory areas (cf. PACT04) or in memories connected externally. After executing the test algorithms, the data is read back before the normal program processing.").

12. Referring to claim 6, Vorbach discloses the first computing unit further comprises a first error indicator and the second computing unit further comprises a second error indicator (From line 40 of column 3, "Therefore, it is sufficient to store the number of the defective PAE and send it to a decoder which controls the states of the multiplexers on the basis of the table given above.").

13. Referring to claim 8, Vorbach discloses the first computing unit is an adder (From line 22 of column 6, "The present invention provides for replacing defective units, which are designed as arithmetic and logic units, for example, but in general may be any desired unit of a chip, with a functional unit.").

14. Referring to claim 10, Vorbach discloses the first computing unit is an arithmetic logic unit (From line 22 of column 6, "The present invention provides for replacing defective units, which are designed as arithmetic and logic units, for example, but in general may be any desired unit of a chip, with a functional unit.").

15. Referring to claim 11, Vorbach discloses a method for providing a fault tolerant computing through a single chip runtime repairable processor, comprising the steps of: connecting a plurality of data registers to a first computing unit through a plurality of data paths (From line 44 of column 12, "PAE: processing array element according to German Patent Application No. 196 51 075.9-53. Although a PAE in German Patent Application No. 196 51 075.9-53 is an arithmetic and logic unit, the term is used in more general terms in the present patent to represent any desired cell, i.e., arithmetic and logic units, state machines, memories, etc." From line 44 of column 11, "Before executing the test algorithms, the internal registers of the cells (1702) are stored in the RAM or RAM area (1701). After execution of the test algorithms, the data is written back into the internal registers of the cells." For example, figure 1, buses 0110 and PAEs 0101.);

defining an area of the chip that covers at most the plurality of the data paths wherein the first computing unit and the plurality of data registers are confined within the area (For example, figure 1, buses 0110 and PAEs 0101.);

placing a second computing unit within the area, wherein the second computing unit being a duplicate of the first computing unit (From line 50 of column 12, "PAER: cell which is additionally implemented on the integrated circuit and can be used as a

replacement for a defective cell of the same design.");

connecting the plurality of data registers to the second computing unit (From line 44 of column 11, "Before executing the test algorithms, the internal registers of the cells (1702) are stored in the RAM or RAM area (1701). After execution of the test algorithms, the data is written back into the internal registers of the cells.");

detecting an error condition in the first computing unit; in response to detecting the error condition, disabling the first computing unit; and in response to disabling the first computing unit, enabling the second computing unit (From line 66 of column 1, "The present invention provides for replacing defective cells with functional cells and reducing rejects. A cell can be replaced either by the test systems at the time of manufacture of the chips or even by the user in the completely assembled system. Test vectors can be generated according to the BIST principle within the chip, or outside the unit according to a new method to save on space and costs. In addition, a possibility of chips automatically repairing defects without requiring any additional external tool is described. All the tests and repairs can be performed during operation of the chips.").

16. Referring to claim 12, Vorbach discloses the disabling step and the enabling step are controlled by a machine state register (Figure 1, 0109.).

17. Referring to claim 13, Vorbach discloses the step of, in response to detecting an error condition, setting a unit swapping indicator in a machine state register (Figure 1, 0109.).

18. Referring to claim 14, Vorbach discloses the step of, in response to detecting an error condition, executing a diagnostic procedure (For example, figure 11.).

19. Referring to claim 18, Vorbach discloses a runtime repairable processor within a single silicon chip, comprising:

means for storing data (From line 44 of column 11, "Before executing the test algorithms, the internal registers of the cells (1702) are stored in the RAM or RAM area (1701). After execution of the test algorithms, the data is written back into the internal registers of the cells.");

a first computing means for performing computations (From line 44 of column 12, "PAE: processing array element according to German Patent Application No. 196 51 075.9-53. Although a PAE in German Patent Application No. 196 51 075.9-53 is an arithmetic and logic unit, the term is used in more general terms in the present patent to represent any desired cell, i.e., arithmetic and logic units, state machines, memories, etc.");

means for devising a plurality of data paths for connecting the means for storing data to the first computing means (For example, figure 1, buses 0110 and PAEs 0101.);

and a second computing means for performing computations, wherein the second computing means is a duplicate of the first computing means and is connected to the means for storing data (From line 50 of column 12, "PAER: cell which is additionally implemented on the integrated circuit and can be used as a replacement for a defective cell of the same design." For example, figure 1, buses 0110 and PAEs 0101.),

the first computing means and the second computing means being placed within

the area defined by at most the means for devising a plurality of data paths (For example, figure 1, buses 0110 and PAEs 0101.).

Claim Rejections - 35 USC § 103

20. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

21. Claim 3, 15, 16 rejected under 35 U.S.C. 103(a) as being unpatentable over US 6697979 to Vorbach et al. as applied to claim 2, 11 above, and further in view of US 7017074 to Okin.

22. Referring to claim 3, 15, 16, Vorbach discloses the PAEs are operated using clocks (From line 57 of column 2, "Depending on the fault tolerance requirements, the clock signal, for example, can be sent over multiplexers to prevent a possible short circuit, or the clock signal may be sent directly to the cell because such a failure need not be compensated."). Although Vorbach does not specifically disclose the control enables/disables a computing unit by enabling/disabling the clock signal to that computing unit, such control is known in the art. An example is shown by Okin from line 55 of column 7, "controller is further configured to cause one or more of the redundant processors to be disabled by disabling a clock signal used to clock the one or more of the redundant processors." A person of ordinary skill in the art at the time of the invention would have been motivated to disable the clock because, as indicated by

Vorbach, there is a need to disable any particular processor and any particular processor has its own clock signal fed to it, and as disclosed by Okin, disabling the clock disables the processor.

23. Claim 7, 17 rejected under 35 U.S.C. 103(a) as being unpatentable over US 6697979 to Vorbach et al. as applied to claim 6, 11 above, and further in view of US 4890285 to Dichiara.

24. Referring to claim 7, 17, Vorbach discloses the first and second error indicators are stored (From line 40 of column 3, "Therefore, it is sufficient to store the number of the defective PAE and send it to a decoder which controls the states of the multiplexers on the basis of the table given above."). Although Vorbach does not specifically disclose that they may be stored in a machine check trap and that a machine check track may be used to initiate a software diagnostic routine, such machine check traps are known in the art. An example is shown by Dichiara, from the abstract, "If the cycle counter reaches the previously loaded value before completion of the test, a machine-check trap occurs allowing the microdiagnostic code RAM to gain control of the test regardless of any error conditions that are present." A person of ordinary skill in the art at the time of the invention would have been motivated to use such a trap because, from line 30 of column 3 of Dichiara, "The special address locates a machine check trap location that contains suitable microcode. The microcode at the machine check trap location is diagnostic microcode and performs the steps for the diagnostic which are necessary to diagnose the error condition. Thus, the use of the counter 12 enables the microdiagnostic code RAM 10 to break the stall and continue microdiagnostics without

the need for console interaction." And further, Vorbach discloses that more testing may be necessary, from line 10 of column 4, "It is not usually sufficient to implement just one test algorithm, but instead multiple different test algorithms may be implemented, each being checked with multiple test vectors. Only in this way can a maximum fault detection rate be achieved."

25. Claim 9 rejected under 35 U.S.C. 103(a) as being unpatentable over US 6697979 to Vorbach as applied to claim 1 above, and further in view of "circular shift" by IEEE dictionary.

26. Referring to claim 9, although Vorbach does not specifically disclose the first computing unit may be a rotator, this is well known in the art. An example of this is shown by "circular shift". A person of ordinary skill in the art at the time of the invention would have been motivated to have a circular shifter because, from line 22 of column 6, "The present invention provides for replacing defective units, which are designed as arithmetic and logic units, for example, but in general may be any desired unit of a chip, with a functional unit." And further the circular shifting of bits is a very well known and motivated operation of the art.

Conclusion

27. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. See notice of references cited.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Gabriel L. Chu whose telephone number is (571) 272-

3656. The examiner can normally be reached on weekdays between 8:30 AM and 5:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Scott Baderman can be reached on (571) 272-3644. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Gabriel L. Chu
Examiner
Art Unit 2114

gc